I claim:

1. A method of exercising a component on an integrated circuit, comprising the steps of:

providing an integrated circuit having an optically sensitive device and a component wherein said optically sensitive device is electrically connected to said component;

connecting the integrated circuit to an electrical source; and

optically stimulating said optically sensitive device so as to allow current to flow through said optically sensitive device from said electrical source to said component so as to exercise said component.

2. The method of claim 1 wherein said electrical source is a power source and wherein said current flow is a positive current flow to said component.

3. The method of claim 1 wherein said electrical source is an electrical ground and wherein said current flow is a negative current flow to said component.

4. The method of claim 1 wherein said optically sensitive device is a diode.

5. The method of claim 1 wherein the step of optically stimulating said optically sensitive device comprises providing a probe

card having an aperture therein, aligning said aperture with said optically sensitive device, and providing a source light beam through said aperture to optically stimulate said optically sensitive device.

6. The method of claim 1 wherein the step of optically stimulating said optically sensitive device comprises providing a filter mask, and activating said filter mask for a predetermined time period to allow passage of a light beam through said filter mask to optically stimulate said optically sensitive device for said predetermined time period.

7. The method of claim 1 wherein the step of providing an integrated circuit comprises providing a wafer having a plurality of integrated circuits thereon.

8. The method of claim 1 wherein the step of optically stimulating said optically sensitive device comprises providing a fiber optic bundle having individual strands therein, aligning at least a selected one of said individual strands with said optically sensitive device, and providing a light beam through said at least a selected one of said individual strands to optically stimulate said optically sensitive device.

9. The method of claim 1 wherein the step of connecting the integrated circuit to an electrical source comprises providing a probe card having an electrical lead connected at a first end to said electrical

source and connected at a second end to an electrically conductive bump, and connecting said electrically conductive bump to said integrated circuit.

10. The method of claim 1 wherein the step of optically stimulating said optically sensitive device comprises providing a probe card having multiple layers therein including a power source layer, an insulation layer and a ground layer, and wherein said probe card further includes an aperture that extends through said multiple layers so as to allow the passage of light through said probe card to said integrated circuit.

11. A device for exercising a component on an integrated circuit, comprising:

a probe card including:

a power source connection electrically connected to an outside power source and electrically connected to a power source contact pad on the integrated circuit during exercising of the integrated circuit;

a ground connection electrically connected to an outside electrical ground and electrically connected to a ground contact pad on the integrated circuit during exercising of the integrated circuit;

an aperture that extends through said probe card and that is aligned with an optically sensitive device on said integrated circuit during exercising of the integrated circuit; and

a light source that provides a beam of light through said aperture so as to optically stimulate said optically sensitive device to exercise said integrated circuit.

12. The device of claim 11 further comprising a filter mask that allows passage of said beam of light through said filter mask for a predetermined time period to optically stimulate said optically sensitive device for said predetermined time period.

13. The device of claim 11 further comprising a fiber optic bundle having individual strands therein, wherein at least a selected one of said individual strands is aligned with said aperture, and wherein said at least a selected one of said individual strands transmits said beam of light from said light source to said aperture.

14. The device of claim 11 wherein said light source is chosen from the group consisting of a light bulb, multiple light bulbs, a laser, multiple lasers, and a liquid crystal display panel.

15. The device of claim 11 further comprising a burn-in chamber containing said probe card and said light source, and further comprising a light control signal, a multi-filter mask, a light channel controller, a fiber optic block, a heating device, and a temperature control device.

16. The device of claim 15 wherein said burn-in chamber further comprises a parabolic reflector, said light control signal comprises a liquid crystal display panel, said multi-filter mask comprises at least one wavelength filter, said light channel controller comprises a computer, said fiber optic block comprises a fiber optic bundle, said heating device comprises heating coils, and said temperature control device comprises an anodized aluminum plate connected to a thermostat.

17. The device of claim 11 wherein said probe card extends across a diameter of a wafer containing multiple integrated circuits thereon and wherein said power source connection of the probe card comprises a power source layer that is connected to a power source contact pad on each of the integrated circuits during exercising of the integrated circuits, wherein said ground connection of the probe card comprises a ground layer that is connected to a ground contact pad on each of the integrated circuits during exercising of the integrated circuits, and wherein said probe card includes multiple apertures that extend through said probe card and are aligned with corresponding ones of an optically sensitive device of each of the integrated circuits during exercising of the integrated circuits.